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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Pankaj K. Jha		
Application No.:	09/881,367	Examiner:	Patel, H.
Filed:	June 14, 2001	Art Group:	2154
For:	PROGRAMMABLE PROTOCOL PROCESSING ENGINE FOR NETWORK PACKET DEVICES		

CERTIFICATE OF MAILING

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 7, 2006.

By: Mary Donna Berkley
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APPEAL BRIEF - REPLACEMENT SECTION

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief regarding 37 CFR 41.37(c)(1)(v), mailed February 21, 2006, Appellant submits the following replacement section V pursuant to 37 C.F.R. §41.37(d) and M.P.E.P. §1205.03 for consideration by the Board of Patent Appeals and Interferences. Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A first embodiment of the present invention (as represented by claim 1) generally concerns a method of bridging (see all of FIG. 2 and page 5, line 7 through page 13, line 15) an incoming packet (page 5, lines 13-18) from a first network 104 to a second network 106. Examples of the first network 104 and the second network 106 are generally described in the specification on page 6, lines 1-11. An example packet is generally illustrated by an Ethernet frame in FIG. 5 and described on page 18, lines 4-6. The method may comprise a first step for (A) reading a pointer (e.g., signal POINTER in FIG. 2, page 12, line 18 through page 13, line 4 and page 13, lines 14-15) for a first parameter (e.g., MAC destination, MAC source, PDI, in FIG. 5 and page 18, lines 5-13) within the incoming packet. Blocks 150 and 152 (see FIG. 4 and page 17, lines 8-15) generally illustrate reading the first parameter off the incoming packet. Once the parameter is found, the pointer may be read in the step 154 as discussed in the text on page 17, lines 4-15. The step for reading may be implemented by a parser circuit 134 (see FIG. 3) as described in the specification on page 14, lines 4-10. The method includes a second step for (B) processing the first parameter in accordance with the pointer to produce a second parameter (e.g., matching address in FIG. 5 and page 18, line 19 through page 19, line 3). The blocks in the bracket 156 (see FIG. 4) generally illustrate several example processing methods based on the pointer. The processing is generally described in the specification on page 17, lines 16-20. The step for processing may be implemented by a number of peripherals 132a-132q (see FIG. 3), as described in the specification on page 14, line 11 through page 15, line 10. The method may include a third step for (C) presenting an outgoing packet (page 5, lines 13-18) containing the second parameter for the second network. Blocks 158, 160 and 162 (see FIG. 4) generally illustrate assembling the outgoing parameter, framing an outgoing frame (page 5, lines 11-15) and then transmitting the outgoing frame, respectfully. The steps 158-162 are

generally described in the specification on page 17, line 20 through page 18, line 3. The step for presenting may be implemented by an assembler circuit 136 as disclosed in the specification on page 15, lines 11-20.

A second embodiment of the present invention (as represented by claim 16) generally concerns a circuit 126 (see all of FIG. 3 and page 11, lines 8-20). The circuit generally comprises (A) a means for reading 134 (see FIG. 3, pages 14, lines 4-10, and FIG. 4 and page 17, lines 4-15) a pointer (e.g., signal POINTER in FIG. 2 , page 12, line 18 through page 13, line 4 and page 13, lines 14-15) for a first parameter (e.g., MAC destination, MAC source, PDI, in FIG. 5 and page 18, lines 5-13) within an incoming packet (page 5, lines 13-18) compliant with a network protocol (page 6, lines 1-11), (B) a means for processing 132a-132q (see FIG. 3, page 14, line 11 through page 15, line 10, page 16, lines 1-17 and FIG. 4 and page 17, lines 16-20) the first parameter in accordance with the pointer to produce a second parameter (e.g., matching address in FIG. 5 and page 18, line 19 through page 19, line 3); and (C) a means for presenting 136 (see FIG. 3, page 15, lines 11-20 and FIG. 4 and page 17, line 20) an outgoing packet (page 5, lines 13-18) containing the second parameter. An example packet is generally illustrated by an Ethernet frame in FIG. 5 and on page 18, lines 4-6. The means for reading may be described in the specification on page 14, lines 4-10 and page 17, lines 4-15 (referring to FIG. 4) . The means for reading may be implemented as a protocol engine 126, a processing circuit 128 and/or a parser circuit 134. The means for processing may be described in the specification on page 14, line 11 through page 15, line 10, page 16, lines 1-17 and page 17, lines 16-20 (referring to FIG. 4) . The means for processing may be implemented as a protocol engine 126, a processing circuit 128, an external peripheral circuit 108, peripheral circuits 132a-132q, dedicated hardware and/or programmable processors. The means for presenting may be described in the specification on page 15, lines 11-20 and page 17, line 20 through page 18,

line 3 (referring to FIG. 4). The means for presenting may be implemented as a protocol engine 126, a processing circuit 128 and/or an assembler circuit 146.

Claim 17 (argued separately) provides a means for partitioning the incoming packets. The means for partitioning may be implemented as a parser circuit 134 (see FIG. 3). The means for partitioning is generally described in the specification on page 14, lines 4-10 and on page 17, lines 8-15 (referring to FIG. 4).

Claim 18 (argued separately) provides a plurality of peripheral means at least one (i) linked to the pointer and (ii) configured to perform a process involving the first parameter. The peripheral means may be implemented as the external peripherals circuit 108 and/or a number of peripheral circuits 132a-132q (see FIG. 3). The peripheral means are generally described in the specification on page 14, line 11 through page 15, line 10, page 17, lines 16-20 (referring to FIG. 4) and page 18, line 4 through page 20, line 4 (referring to FIG. 5). Example processes are generally described in the specification on page 14, line 11 through page 15, line 10.

Claims 19 and 20 (argued together) provide (i) a first plurality of the peripheral means internal to means for processing, (ii) a second plurality of the peripheral means external to the means for processing and (iii) a means for interfacing to the first network configured to de-frame in compliance with a plurality of network protocols. The first plurality of the peripheral means may be implemented by a number of the peripheral circuit 132a-132m (see FIG. 3). The second plurality of the peripheral means may be implemented by a number of the peripheral circuit 132n-132q and/or the external peripherals circuit 108. The peripheral means are generally described in the specification on page 14, line 11 through page 15, line 10, page 17, lines 16-20 (referring to FIG. 4) and page 18, line 4 through page 20, line 4 (referring to FIG. 5). The means for interfacing may be implemented by a network interface circuit 122 (see FIG. 2) and/or one or more de-frame circuits

188 (see FIG. 6). The means for interfacing is generally described in the specification on page 9, line 18 through page 10, line 3, page 10, line 12 through page 11, line 7, page 17, lines 6-8 (referring to FIG. 4) and page 21, lines 3-16 (referring to FIG. 6) .

Respectfully submitted,

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